In the Specification:

Please amend the paragraph beginning on page 2, line 26 as follows:

Turning now to FIG. 1, a pseudo-NMOS circuit in accordance with one embodiment of the present invention is indicated generally at 10 and includes a load PFET (or PMOS) 12 having a gate 14 tied to ground (GND) so that the PFET is always ON. A source 16 of the load PFET 12 is connected to the supply voltage (VDD), and a drain 18 is connected to a "pulldown" NFET tree or circuit 20 at an output node Z of the pseudo-NMOS circuit 10. The NFET tree 20 is also connected to ground GND. The NFET tree 20 implements the desired equation of the pseudo-NMOS logic 10 and produces the result at the output node Z.

Please amend the paragraph beginning on page 3, line 6 as follows:

A feedback PFET (or PMOS) is also connected between VDD and the NFET tree 20, parallel to the load PFET 12. A source 24 and a drain 26 of the feedback PFET 22 are connected respectively to VDD and the ~~ouput~~ output node Z, as with the load PFET 12. A gate 28 of the feedback PFET 22, however, is connected to an output node FB of an inverter circuit 30.